

Military-Grade Isolated 3-Phase PFC Module

3-Phase 115 Vrms L-N or 270 VDC Input Voltage	0 to 800 Hz Input Frequency	4250 V Isolation	28 Vdc Output Voltage	750W Output Power	100 °C Baseplate Temp	>0.99 PF	1.5% THD	92.0% Full Load Efficiency
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The MilCOTS 3-Phase AC or DC input MPFICQor Isolated Power Factor Correction module is an essential building block of an AC-DC or DC-DC power supply running from a source as defined by MIL-STD-704. It rejects voltage fluctuations from both AC and DC sources and provides Power Factor Correction when operated from an AC source. The MPFIC also rejects pulsed loads, preventing large load transients from being passed back to the AC or DC source. It is designed to comply with a wide range of military standards and is manufactured in the United States.

MPFICQor[™]



Designed and manufactured in the USA

Operational Features

- Compatible with Military Standard 60 Hz, 400 Hz & var. freq. systems
- Compatible with Military Standard 270 Vdc sources
- Harmonic content meets military standards
- Enables systems with repetitive load transients to pass MIL-STD-461 CE101 requirement by offering superior load current rejection
- Minimal inrush current
- Balanced phase currents
- High power factor (0.99 at 400 Hz / 750 W)
- Minimal external output capacitance requirement
- Supports full load current during startup ramp
- Ability to meet full EMI with available additional EMI filters
- N * 750 W power levels when paralleled

Mechanical Features

- Industry standard Full-brick-size
- Size: 2.486" x 4.686" x 0.512" (63.14 x 119.02 x 13.0 mm)
- Weight: 10.0 oz (284 g)

Protection Features

- Output current limit and auto-recovery short circuit protection
- Auto-recovery input under/over-voltage protection
- Auto-recovery output over-voltage protection
- Auto-recovery thermal shutdown

Safety Features

- (Pending)
- Input/Output to baseplate isolation 2150Vdc
 - CE Marked

Control Features

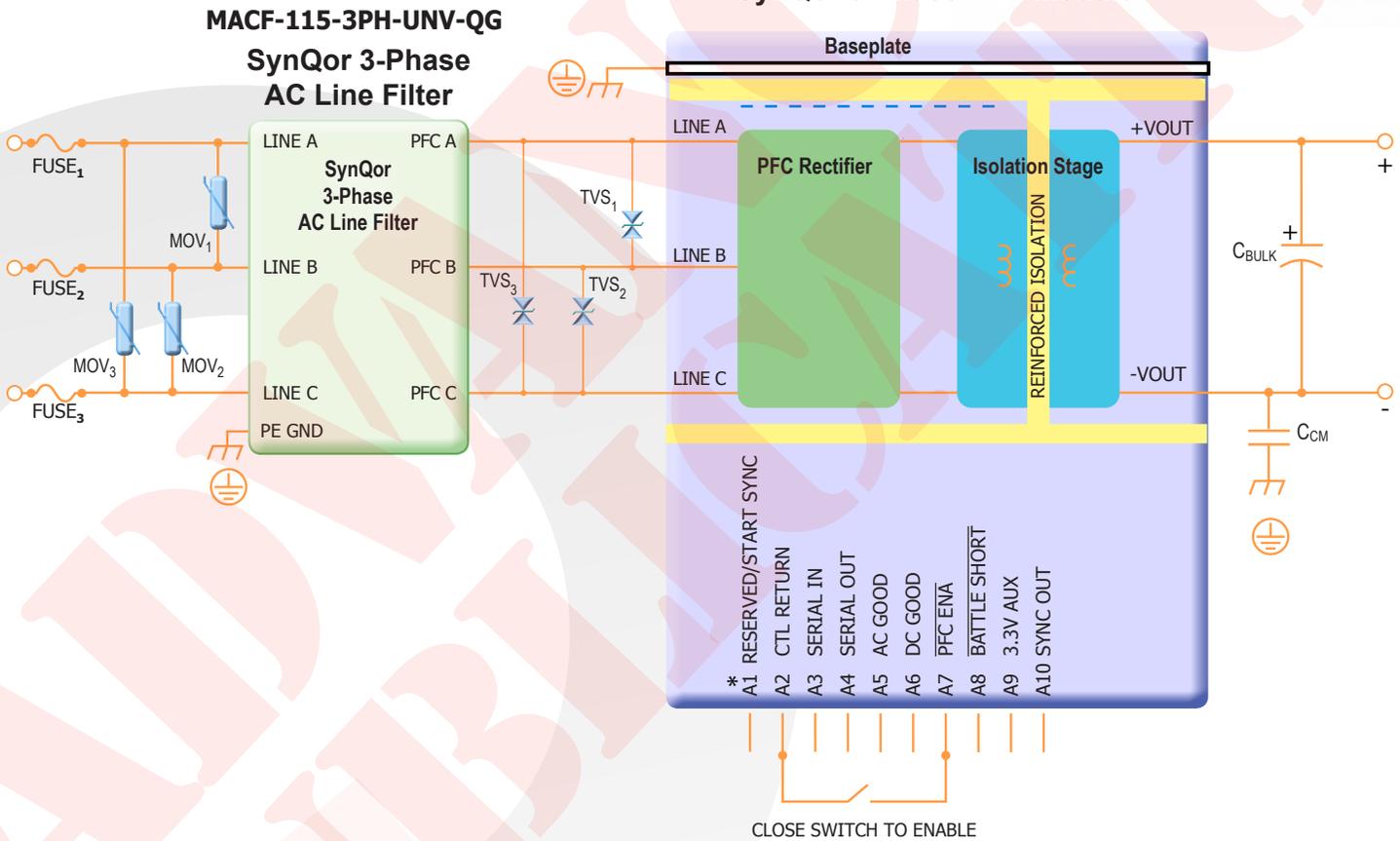
- All control pins referenced to separate floating return
- Asynchronous serial data interface
- Input and and Ouput Power Good outputs
- MPFIC Enable and Battle Short inputs
- 3.3 V always-on standby power output
- Clock synchronization output

Compliance Features

- MIL-STD-704 (A-F)
- MIL-STD-461 (C, D, E, F)
- MIL-STD-1399 (at 200 Vrms L-L)
- MIL-STD-810G
- RTCA/DO-160

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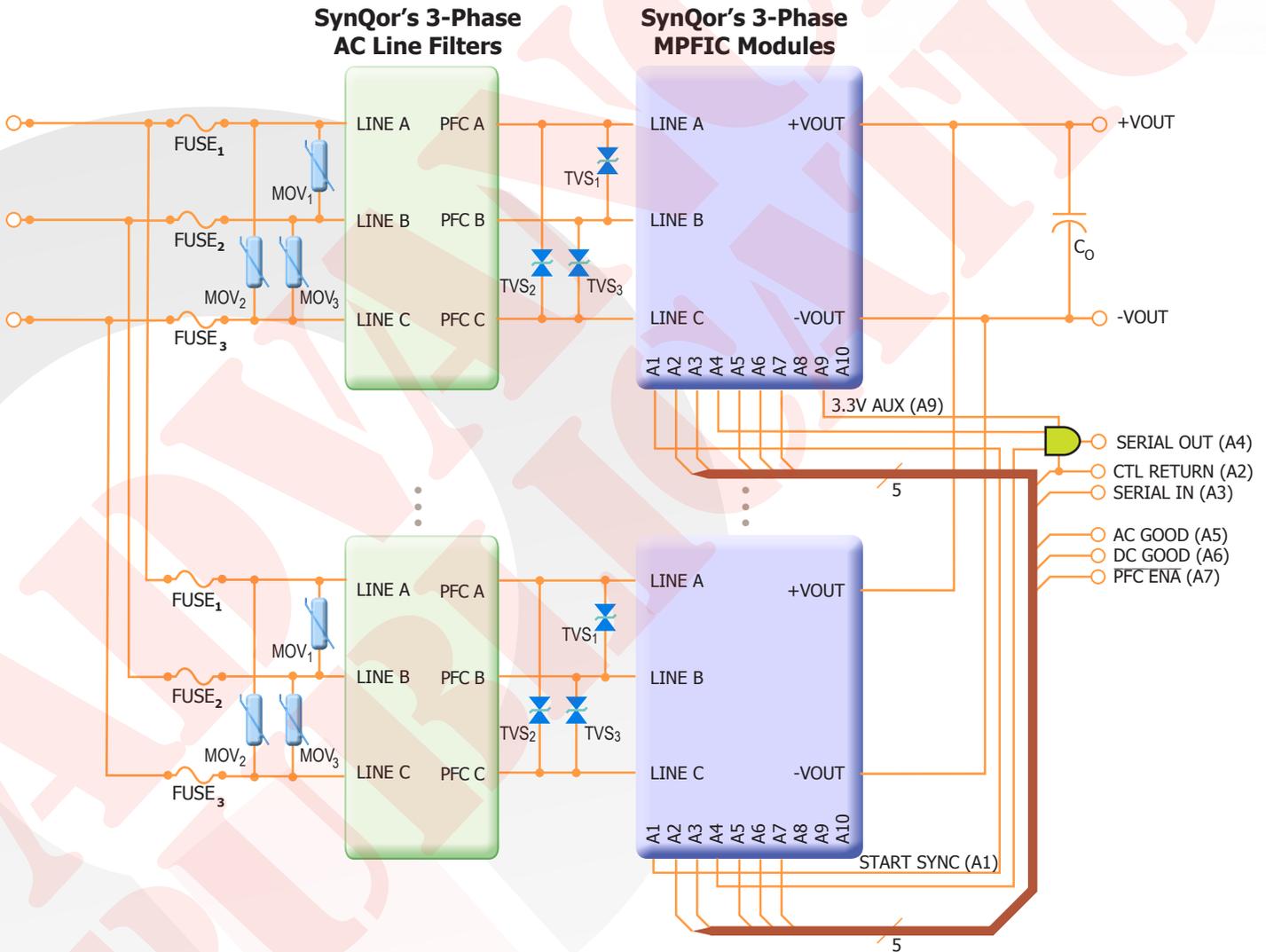


* Note A1 RESERVED for Regulated Module
START SYNC for Droop Module

Suggested Parts:

MOV₁₋₃: 300 Vrms, 60 J; EPCOS S10K300E2
TVS₁₋₃: 430 Vpk, 20 J; Littelfuse AK3-430C or Bourns PTVS-430C-TH
Fuse₁₋₃: 250 Vrms, 10 A; Littelfuse 0216010.XEP

Figure A: Typical application of the Isolated PFCQor module



Suggested Parts:

- MOV₁₋₃: 300 Vrms, 60 J; EPCOS S10K300E2
- TVS₁₋₃: 430 Vpk, 20 J; Littelfuse AK3-430C or Bourns PTVS-430C-TH
- Fuse₁₋₃: 250 Vrms, 10 A; Littelfuse 0216010.XEP

Figure B: Typical application with multiple Isolated PFCQor modules wired in parallel

MPFIC-115-3PD-28x-FT Electrical Characteristics

Operating Conditions: 115 Vrms L-N (199 Vrms L-L) 3-Phase 400 Hz; 750W output; baseplate temperature = 25 °C; output capacitance = 2.6mF unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C. Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
ABSOLUTE MAXIMUM RATINGS					
Input Voltage			575	Vpk L-L	Differential across any two line inputs
SERIAL IN and PFC ENA inputs	-2		7	V	Relative to CTL RETURN pin
AC GOOD, DC GOOD, and BATTLE SHORT outputs					
Pull Up Voltage	-2		7	V	Relative to CTL RETURN pin
Sink Current			10	mA	
Operating Temperature	-55		100	°C	Baseplate temperature
Storage Temperature	-65		135	°C	
INPUT CHARACTERISTICS					
Input Voltage Range, Operating					See app section "Power Ratings"
Continuous	100		140	Vrms L-N	173 to 242 Vrms L-L
Transient (≤ 1 s)	240		350	Vdc	
	60		180	Vrms L-N	104 to 312 Vrms L-L
	147		440	Vdc	
Input Overvoltage Protection (Between any two line inputs)	485	500		Vpk L-L	Threshold levels guaranteed by design
Operating Input Frequency	0		800	Hz	
Source Inductance			2	mH	per Phase
Recommended Operating Range with Line Imbalance					
Amplitude Imbalance			5	Vrms L-N	
Phase Imbalance			5	deg	
Thresholds for Phase Drop Warning & Shutdown					Warning causes BATTLE SHORT pin to go high
Amplitude Imbalance		37		Vrms L-N	0.25s shutdown delay
Phase Imbalance		18		deg	
Inrush of AC Input Current			5	A	Output cap is charged later during startup ramp
Power Factor		0.99			
Reactive Power (per phase)					See note 1. Scales with AC line frequency.
400 Hz, Zero load or Disabled;		45		VAR	Leading
400 Hz, Pout > 250 W		0		VAR	See app section "Reactive Power at Fundamental"
Total Harmonic Distortion of AC Input Current		1.5	2.5	%	Full load (see Figure 4 for data vs. load)
Enabled AC Input Power, No Load (sum of phases)					
400Hz		16		W	
60Hz		14		W	
Disabled AC Input Power (sum of phases)					
400Hz		6		W	
60Hz		4		W	
Input Current Imbalance			±1	%	
Maximum Input Current (per phase)			3	Arms	Provided for rating of circuit / fuse
ISOLATED OUTPUT CHARACTERISTICS					
Output Steady-State Voltage	27.5	28.0	28.5	V	Zero Load
Output Voltage Droop					
Regulated Model		-0.5		V	Full Load, see Figure 9
Droop Model		-2		V	Full Load, see Figure 9
Operating Output Current Range	0		27	A	
Output Current Limit			36	A	
Output Steady-State Voltage Ripple			84	mVrms	With minimum +VOUT capacitance and balanced line
Recommended Output Capacitance	2.3		50	mF	Use R D for additional cap
Output Over-Voltage Limit Threshold (Full Temp Range)	31		39	V	Not tested, guaranteed by design
EFFICIENCY					
100% Load (750W)		92.0		%	400 Hz (0.3% higher at 60 Hz)
50% Load (375W)		92.5		%	400 Hz (0.5% higher at 60 Hz)
DYNAMIC CHARACTERISTICS					
Turn-On Transient					
Startup Delay Time		45		ms	From PFC ENA to 10% nominal VOUT, see Figure 19
Total Turn-On Time		500		ms	From PFC ENA to DC GOOD, see Figure 19
VOUT Overshoot			1	%	
Auto-Restart Time		1		s	See "Protection Features" in application section
RELIABILITY CHARACTERISTICS					
Calculated MTBF (MIL-217) MIL-HDBK-217F		549		10 ³ Hrs.	Ground Benign, Tb = 70 °C
Calculated MTBF (MIL-217) MIL-HDBK-217F		85		10 ³ Hrs.	Ground Mobile, Tb = 70 °C
Field Demonstrated MTBF				10 ³ Hrs.	See our website for details

Note 1: Includes contribution from MACF-115-3PH-UNV-QG EMI filter

Technical Specification

MPFIC-115-3PD-28x-FT Electrical Characteristics (continued)

Operating Conditions: 115 Vrms L-N (199 Vrms L-L) 3-Phase 400 Hz; 750W output; baseplate temperature = 25 °C; output capacitance = 2.6mF unless otherwise noted. Full operating baseplate temperature range is -55 °C to +100 °C. Specifications subject to change without notice.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
FEATURE CHARACTERISTICS					
SERIAL IN					
Idle / Stop State Input Voltage	2.4			V	
Zero / Start State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
SERIAL OUT					
Idle / Stop State Output Voltage	2.9	3.1		V	4 mA source current
Zero / Start State Output Voltage		0.2	0.4	V	4 mA sink current
INPUT GOOD (positive logic)					
Input Voltage Low Threshold	90	95	100	Vrms L-N	Startup inhibited until INPUT GOOD output high
	220	230	240	Vdc	INPUT GOOD low below this threshold
Input Voltage High Threshold	145	150	155	Vrms L-N	INPUT GOOD low above this threshold
	350	367	380	Vdc	
Hysteresis of Input Voltage Thresholds		1		Vrms L-N	Raises low threshold and lowers high threshold
Line Frequency Low Threshold	-	-	-	Hz	No minimum frequency, MPFIC runs from DC
Line Frequency High Threshold	860	900	940	Hz	INPUT GOOD low above this threshold
Hysteresis of Line Frequency Thresholds		0		Hz	
Low State Output Voltage		0.2	0.4	V	2 mA sink current
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
DC GOOD (positive logic)					
Rising threshold		25		V	DC Power Good output
Falling threshold		18		V	DC GOOD high above this threshold
Low State Output Voltage		0.2	0.4	V	DC GOOD low below this threshold
Internal Pull-Up Voltage		3.3		V	2 mA sink current
Internal Pull-Up Resistance		10		kΩ	
PFC ENA (negative logic)					
Off State Input Voltage	2.4			V	PFC enable input (pull low to enable unit)
On State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
BATTLE SHORT (negative logic)					
Normal State Input Voltage	2.4			V	Battle short input (pull low to disable protection)
Protection-Disabled State Input Voltage			0.8	V	
Internal Pull-Up Voltage		3.3		V	
Internal Pull-Up Resistance		10		kΩ	
3.3V AUX					
Output Voltage Range	3.19	3.30	3.43	V	3.3 V output always on regardless of PFC ENA state
Source Current			100	mA	Over line, load, temp, and life
SYNC OUT					
High State Output Voltage	2.9	3.1		V	Synchronization output at switching frequency
Low State Output Voltage		0.2	0.4	V	4 mA source current
Switching Frequency	190	196.5	203	kHz	4 mA sink current
ISOLATION CHARACTERISTICS					
Any pin to Baseplate					
Pins 2, 3, & 4 to Pins 7 & 9			2150	Vdc	Basic Isolation
Pins 2, 3, & 4 to Isolated Control Pins			4250	Vdc	Reinforced Isolation
Capacitance					
Pins 2, 3, & 4 to Baseplate		1		nF	
Pins 2, 3, & 4 to Pins 7 & 9		1		nF	
Isolation Resistance					
		100		MΩ	
TEMPERATURE LIMITS FOR POWER DERATING CURVES					
Semiconductor Junction Temperature			125	°C	
Board Temperature			125	°C	
Transformer Temperature			125	°C	
Maximum Baseplate Temperature, Tb			100	°C	
Over-Temperature Protection					
Disable Threshold		125		°C	Measured at surface of internal PCB
Warning Threshold		120		°C	Warning causes BATTLE SHORT pin to go high
Enable Threshold		120		°C	



SynQor[®]

Mil-STD-810G Qualification

MPFIC-115-3PD-28x-FT
Input: 3Φ 115Vrms (L-N) or 270 Vdc
Output: 28 Vdc
Power: 750W

Mil-COTS MIL-STD-810G Qualification Testing

MIL-STD-810G Test	Method	Description
Fungus	508.6	Table 508.6-I
Altitude	500.5 - Procedure I	Storage: 70,000 ft / 2 hr duration
	500.5 - Procedure II	Operating: 70,000 ft / 2 hr duration; Ambient Temperature
Rapid Decompression	500.5 - Procedure III	Storage: 8,000 ft to 40,000 ft
Acceleration	513.6 - Procedure II	Operating: 15 g
Salt Fog	509.5	Storage
High Temperature	501.5 - Procedure I	Storage: 135 °C / 3 hrs
	501.5 - Procedure II	Operating: 100 °C / 3 hrs
Low Temperature	502.5 - Procedure I	Storage: -65 °C / 4 hrs
	502.5 - Procedure II	Operating: -55 °C / 3 hrs
Temperature Shock	503.5 - Procedure I - C	Storage: -65 °C to 135 °C; 12 cycles
Rain	506.5 - Procedure I	Wind Blown Rain
Immersion	512.5 - Procedure I	Non-Operating
Humidity	507.5 - Procedure II	Aggravated cycle @ 95% RH (Figure 507.5-7 aggravated temp - humidity cycle, 15 cycles)
Random Vibration	514.6 - Procedure I	10 - 2000 Hz, PSD level of 1.5 g ² /Hz (54.6 g _{rms}), duration = 1 hr/axis
Shock	516.6 - Procedure I	20 g peak, 11 ms, Functional Shock (Operating no load) (saw tooth)
	516.6 - Procedure VI	Bench Handling Shock
Sinusoidal vibration	514.6 - Category 14	Rotary wing aircraft - helicopter, 4 hrs/axis, 20 g (sine sweep from 10 - 500 Hz)
Sand and Dust	510.5 - Procedure I	Blowing Dust
	510.5 - Procedure II	Blowing Sand

Mil-COTS Converter and Filter Screening

Screening	Process Description	S-Grade	M-Grade
Baseplate Operating Temperature		-55 °C to +100 °C	-55 °C to +100 °C
Storage Temperature		-65 °C to +135 °C	-65 °C to +135 °C
Pre-Cap Inspection	IPC-A-610, Class III	•	•
Temperature Cycling	MIL-STD-883F, Method 1010, Condition B, 10 Cycles		•
Burn-In	100 °C Baseplate	12 Hours	96 Hours
Final Electrical Test	100%	25 °C	-55 °C, +25 °C, +100 °C
Final Visual Inspection	MIL-STD-883F, Method 2009	•	•



Application Section

POWER TOPOLOGY OVERVIEW

As seen in Figure A on page 2, this PFC rectifier takes nominal 115 Vrms (L-N) / 199 Vrms (L-L) 3-phase delta AC, or nominal 270 Vdc, at its LINE A/B/C inputs, and uses an active-PFC buck converter and a Bus Converter to create a regulated isolated DC output. This is a true 3-phase rectifier topology, as opposed to a composite of three single-phase rectifiers. A boost converter between the active PFC and the bus converter's input supports the output during input line sags and brownouts.

The term "line-to-neutral (L-N) voltage" is used in this document even though this converter does not utilize a neutral wire. If a neutral wire is present in the application, it should not be connected to the PFC.

PERFORMANCE

Efficiency and Power Dissipation

The efficiency of the converter at 270VDC and 115VAC is shown in Figure 1, the corresponding power dissipation is shown in Figure 2.

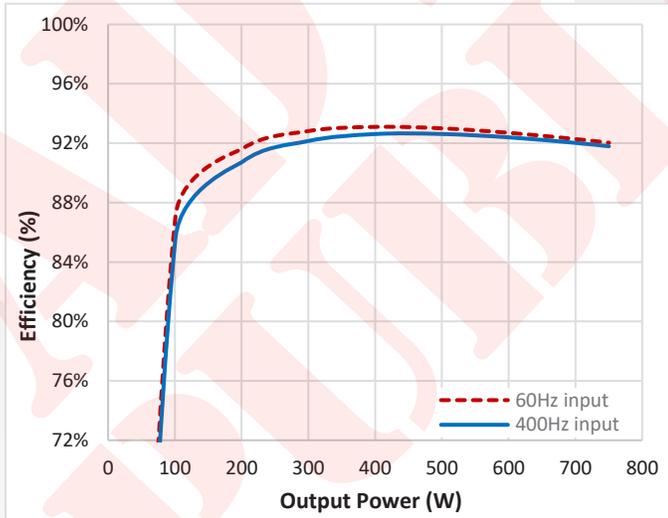


Figure 1: Efficiency vs. output power. Input: 3-phase 115 Vrms (L-N). Baseplate temperature: 30 °C.

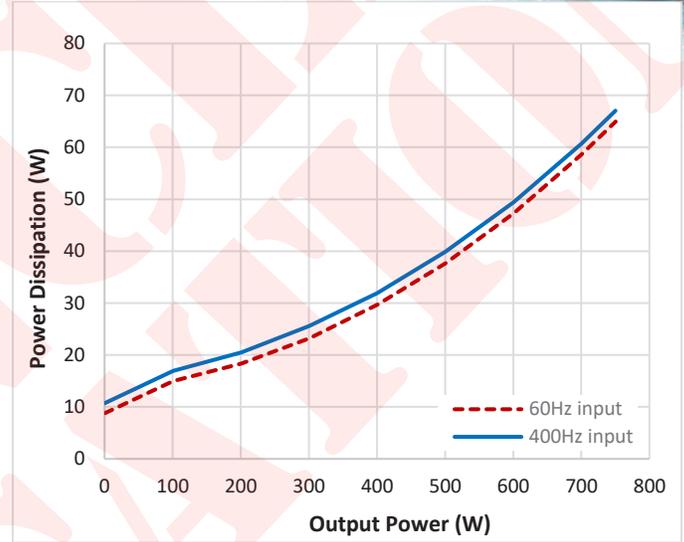


Figure 2: Power dissipation vs. output power. Input: 3-phase 115 Vrms (L-N). Baseplate temperature: 30 °C.

The efficiency and dissipation are identical with 270VDC or 60Hz AC inputs; with a 400Hz AC input, the dissipation increases about 1.5W, due to the increased (reactive) currents in the input filter damping elements.

Input Current Distortion & Harmonics

Legacy diode rectifier solutions typically use bulky magnetics, while having relatively high distortion at line harmonics. In contrast, this modern PFC rectifier switches at high frequency, providing for very low distortion while using small and light internal magnetics. Active current control yields low harmonic content and well-balanced phase currents, even with phase and/or amplitude imbalance on the line inputs.

Input current harmonic content is minimal above 25% of full rated output power, increasing somewhat at light loads due to

buck converter discontinuous mode operation (see Figure 3). Input current THD will increase with higher input voltage.

below 25% load is the leading current due to the filter capacitors evident.

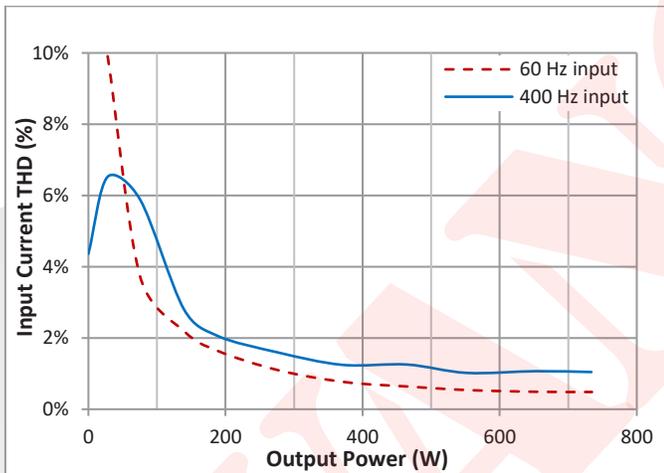


Figure 3: Input Current THD over full load range at 115 Vrms (L-N). Includes external input filter module, part number MACF 115 3PH-UNV QG.

Typical 400Hz line-current harmonics at full power are shown in Figure 4. All are more than 40dB below the fundamental, and indeed, except for the 5th, all are below the 10mA “disregard” threshold of RTCA DO-160G section 16.7.1.

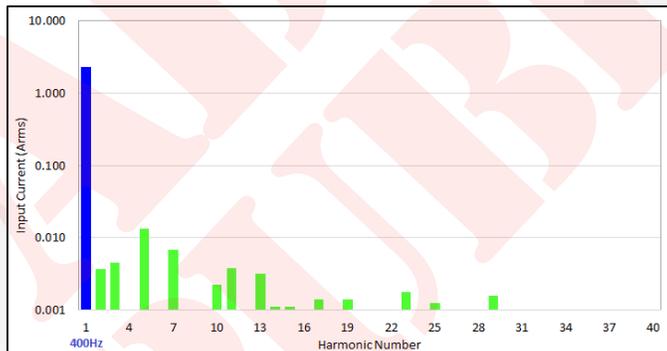


Figure 4: Typical input-current harmonic content. 115 Vrms (L-N) 400Hz, 750W out.

Reactive Power at Fundamental

Line capacitance is necessarily integral to the input EMI filter circuitry, which is divided between internal filtering and the external MACF-115-3PH-UNV-QG input filter module. Total leading reactive power (including that of the external input filter module) scales with line frequency; it is approximately 45 VAR (300mA rms) per phase at 115V rms, 400 Hz.

At all but light loads, however, the PFC actively draws currents that lag input voltage slightly – to cancel the VAR of all the input filter capacitors. This can be seen directly in Figure 5, where, even at 400Hz, at 50% load and above, the input current is in phase with the applied input voltage. Only

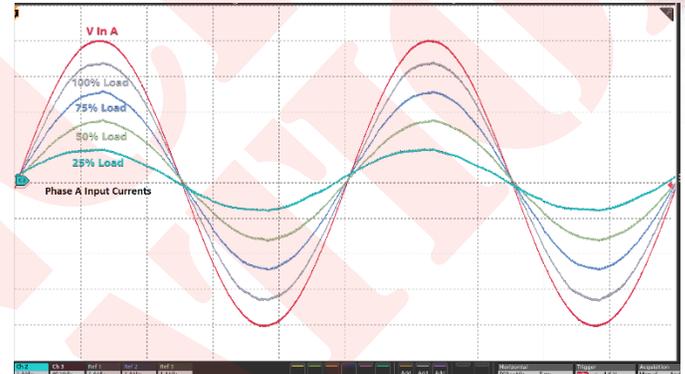


Figure 5: Typical 400 Hz input current waveforms (only Phase A shown); includes MACF-115-3PH-UNV-QG external input filter module.

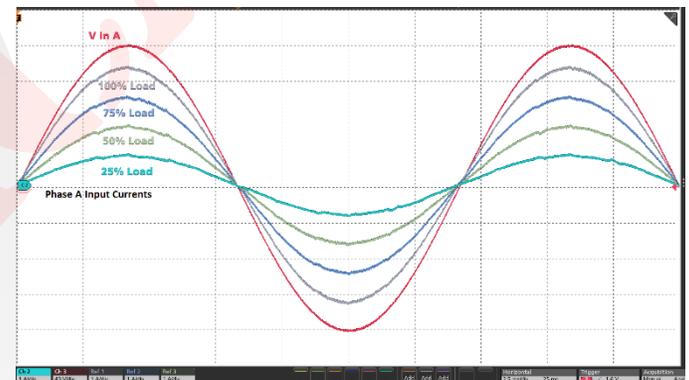


Figure 6: Typical 60 Hz input current waveforms (only Phase A shown); includes MACF 115 3PH-UNV QG external input filter module.

Figure 6 further shows that at 60Hz, input currents are in phase with input voltage at all power levels above 25%.

Both these results are also illustrated in Figure 7 as leading power factor vs. output power at both 400Hz and 60Hz.

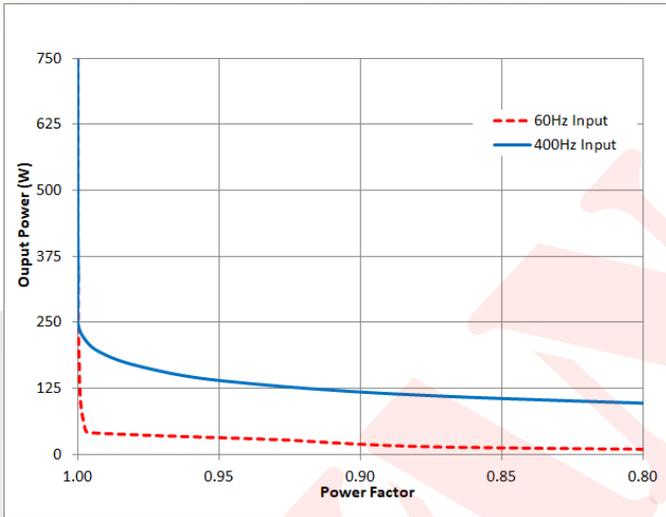


Figure 7: Input leading power factor as a function of operating power level; includes MACF-115-3PH-UNV-QG external input filter module.

At 60Hz, the power factor is essentially unity for all power levels above 50W, while at 400Hz it exceeds 0.95 above 150W and reaches unity at 250W.

POWER CIRCUITRY OVERVIEW

Inrush and Startup

Only a small amount of EMI capacitance resides before the main switches. The PFC buck topology affords excellent control over startup current. Even very large holdup capacitors can be charged gracefully with an actively controlled current limit (see Figure 8).

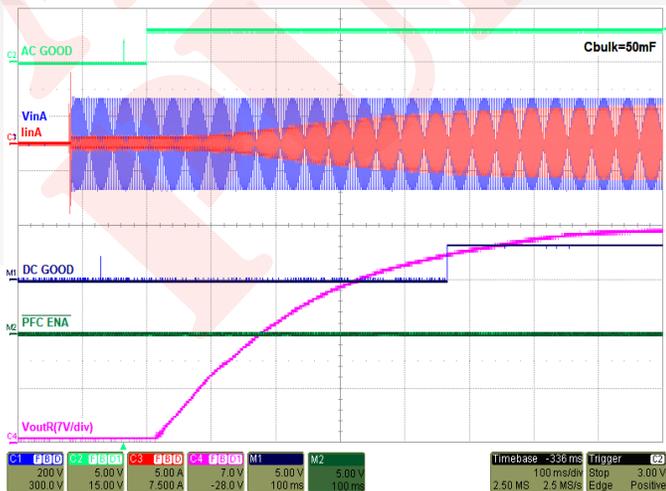


Figure 8: Full-Load (Resistive) startup into 50mF, (for clarity, only Phase A of the input voltage and current are shown).

Startup will only proceed after the INPUT GOOD signal is high. The unit will turn on when all three of the following conditions are met:

- 1) the PFC ENA pin is pulled low
- 2) the input voltage is 100 Vrms (L-N) - 140 Vrms (L-N)
- 3) the input frequency is below 800 Hz

Line Transients

The input stage blocks even severe line transients from reaching the output, allowing generous headroom above typical operating input voltage levels. To both keep input current distortion low and facilitate operation from inductive sources, the input impedance is designed to be resistive down to 2 ms timescales. Figure 9 shows the input current response to an input line-voltage step from 115 Vrms to 140 Vrms and back to 115Vrms. The resistive input characteristic requires that the unit initially increase its current draw in response to the increased voltage. As can be seen in the envelope of the currents, this results in a 2ms slug of energy being transferred from the input to the bulk cap at the output.

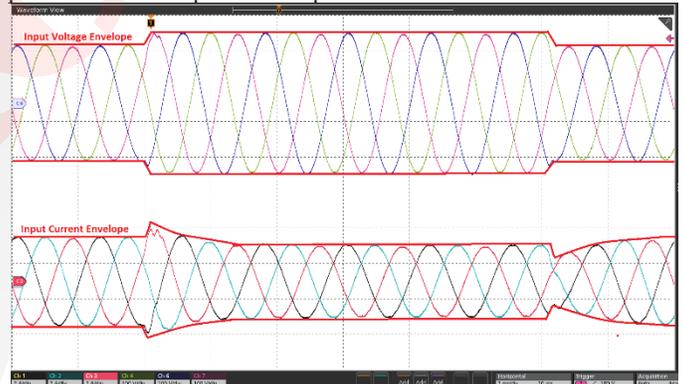


Figure 9: Input current response to a 115 to 140 Vrms and back line voltage transient. 400Hz, 75% output power, 2ms/div.

Line Frequency and Phase Rotation

The PFC does not use an internal phase-locked loop, allowing seamless fast input frequency transients over the full operating range.

The unit operates equally well with either ABC or CBA input voltage phase rotation. If Line Frequency is queried over the serial interface, the returned value will be positive for ABC rotation, negative for CBA rotation, and zero if supplied from 270VDC.

AC Line Brownouts

The PFC can regulate its output indefinitely over the continuous operating range of 100 < Vin < 140 Vrms. When Vin dips below 100 Vrms, or 210 Vdc, an internal boost converter runs briefly to keep the output in regulation. The boost can run for a few seconds (the actual time is determined by line voltage, load, and temperature), after which it is disabled and the output

voltage falls to the steady-state value. This behavior is illustrated in Figure 10.

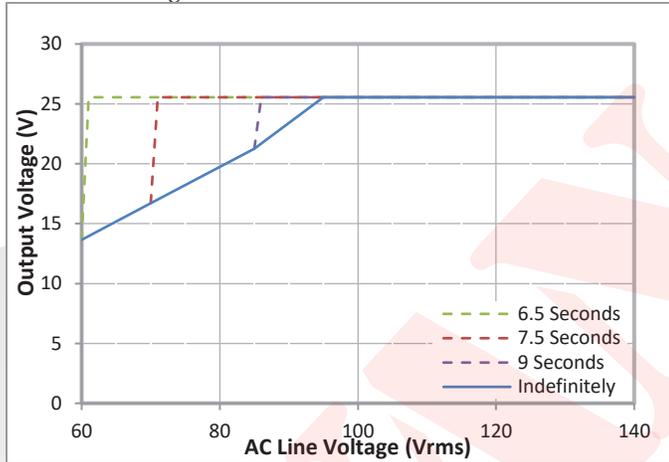


Figure 10: Full Load Output Voltage during Line Brownouts

VOU Regulation and Droop

The MPFIC-115-3PH-28x-FT converter is available with two output voltage control choices: Regulated (x=R), and Droop (x=D). The regulated model is intended for standalone applications where tight control of the nominal voltage is desired. The Droop model is intended for sharing applications. In both, the output is tightly regulated at no-load, but in the droop model, the output voltage is programmed to decrease with increased load current (see Figure 11).

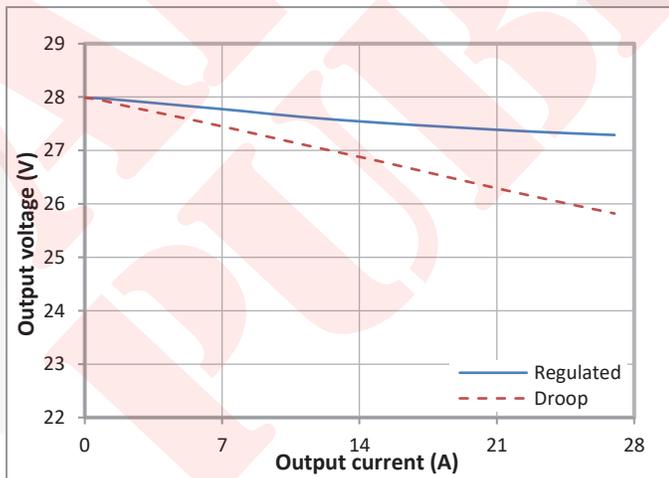


Figure 11: Steady-State Output Voltage vs. Output Current characteristics for both Regulated and Controlled Droop models.

VOU Load Transient Response

To maintain low distortion and harmonic content of the input currents, the regulation response of the both Regulated and Droop models is intentionally quite slow; the recovery time constant from load transients is about 100 ms. Higher-speed

load transients must be handled by output capacitance and downstream converters. Figure 12 illustrates the devices' load transient responses.

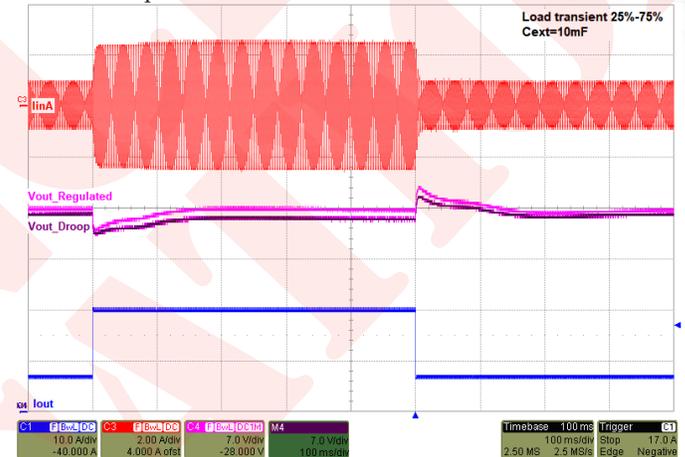


Figure 12: Responses to 25%-75%-25% Load Transient Steps: Cext=10mF, both Regulated and Droop models.

PARALLELING GUIDELINES

The droop version of the PFC modules includes several control features to facilitate paralleling. Up to 10 units may be paralleled with outputs directly connected. A typical application schematic for direct paralleling is shown in Figure B. Current sharing is achieved via the output voltage droop characteristic shown in Figure 11. This sharing method is inherently simple and robust: it is distributed (no master/slave), and involves no communication between units.

Reverse Power Flow

Because each switch in the PFC Rectifier is connected in series with a high-voltage diode, reverse power flow (from the device's output back into the AC input) is prevented. This protection exists in all modes of operation: disabled, starting up, operating and shutting down – and it allows PFC units to be paralleled without the concern for backdrive or circulation currents.

Current Sharing Accuracy

The output voltage is controlled to vary significantly as a computed function of measured current (see Figure 11). The voltage offset and gain is factory calibrated to minimize unit-to-unit variation. This calibration process results in good sharing accuracy: the output power of each unit typically matches the average power to within +/- 50 W. External output wiring resistances should be matched between units for optimum sharing performance.

Features for *Paralleling* (Droop)

Several special features are included to facilitate paralleling:

- 1) When connected between multiple units, the START SYNC bus actively aligns the restart time between units following an event that causes units to enter hiccup-mode. For instance, when full load is applied, one or more units could experience over-temperature shutdown, causing the remaining units to engage current limit, and 50 ms later entering hiccup due to midbus under-voltage shutdown. When these units attempt to restart, they may not start because some units are still forced off due to high temperature and the remaining units cannot support full load. When all the units are cool enough to restart, the hiccup times between all units will probably not be aligned, so without START SYNC, the system may still not start. The START SYNC feature delays restart until all units are out of the hiccup state, so that all units will start up simultaneously.
- 2) The “E” serial port command automatically assigns a unique “Net Address” to each unit in the system. All units must be disabled at the time this command is issued. Each unit has a unique 120-bit number stored in ROM, which is encoded onto the START SYNC bus during this enumeration process. The resulting assigned “Net Address” may be used with a shared serial port to communicate individually to each unit in a paralleled system. The “Net Address” reverts to the default value of ‘m’ when power is cycled, so the enumeration command should be part of the system boot sequence.
- 3) The “N” serial port command optionally overrides the state of the $\overline{\text{PFC ENA}}$ input, allowing a unit to be forced on or off.
- 4) The Battle-Short function may be set via the serial port using the “n” command.

Control Connections for Paralleling

The following are control signal wiring recommendations for a parallel system:

- 1) The CTL RETURN pins from multiple units should be connected together to provide a common control ground.
- 2) SERIAL IN and $\overline{\text{PFC ENA}}$ input pins may be wired in parallel.
- 3) AC GOOD and DC GOOD output pins may be wired in parallel.
- 4) START SYNC should be connected in parallel between all units in the system.
- 5) The 3.3V AUX outputs could also be paralleled, but total current drawn from 3.3VAUX should not exceed the 100 mA rating of a single unit.
- 6) SYNC OUT pins should not be connected between units: doing so would cause a logic output contention.

- 7) The SERIAL OUT signals may be combined using an external AND gate. Alternatively, a multi-drop bus may be formed by pulling the bus low when SERIAL OUT is low, and releasing the bus when SERIAL OUT is high, returning the bus to the idle state via a pull-up resistor. The time constant of this pull-up resistor along with any parasitic capacitance must be much shorter than the baud rate.
- 8) $\overline{\text{BATTLE SHORT}}$ pins should not be interconnected between units. When not warning of an impending shutdown, the $\overline{\text{BATTLE SHORT}}$ pin is normally pulled low, and this could erroneously cause other units to enter the Battle-Short state. If the $\overline{\text{BATTLE SHORT}}$ protection-warning output function is used in a paralleled system, then individual signals should be combined using an OR gate. If the $\overline{\text{BATTLE SHORT}}$ protection-disable input function is used in a paralleled system, then either a separate pull-down transistor should be used for each unit, or the Battle-Short function may be accessed via the serial port. If a $\overline{\text{BATTLE SHORT}}$ pin is not used, it may be left open.

Power Connections for Paralleling

The following are power wiring recommendations for a parallel system:

- 1) +VOUT and -VOUT may be wired directly in parallel.
- 2) The LINE A/B/C inputs should be wired in parallel upstream of their individual input filters. Do not wire individual EMI filters directly in parallel at both their inputs and their outputs.
- 3) Each PFC unit should have its own TVS bank located near the input pins.

POWER INPUT PINS

Operation from AC Power

115 Vrms (L-N) 3-Phase AC input power is applied to the LINE A, LINE B, and LINE C input pins. The direction of phase rotation (ABC or CBA) does not matter; the inputs can be connected in any order desired.

Again, if Line Frequency is queried over the serial interface, the returned value will be positive for ABC rotation, negative for CBA rotation, and zero if supplied from 270VDC.

Operation from DC Power

While 270 Vdc power *can* be applied to the LINE A, LINE B, and LINE C input pins in any connection desired (without concern for polarity) the best thermal performance is obtained when +270VDC is applied to the LINE A and LINE B inputs and 270VDC return is connected to the LINE C input.

The MACF-115-3PH-UNV-QG 3-phase input filter can also be employed with 270 Vdc power. DC polarity is again irrelevant, and slightly higher efficiency will result by connecting two of the filter input & outputs together to one side of the 270 Vdc source.

POWER RATINGS

Thermal Management

Advanced thermal management techniques are employed to create a very low thermal resistance from power devices to baseplate, while retaining SynQor's standard SMT construction and mechanically compliant potting compound. The maximum operating baseplate temperature is 100 °C. Refer to the thermal derating curve, Figure 13, to see the available output current at baseplate temperatures below 100 °C. Operating from a DC source, however, requires limiting the output power at baseplate temperatures above TBD°C, as shown in Figure 13 to keep internal temperatures below 125°C.

DATA TBD

Figure 13: Thermal derating curves for both 115 Vrms (L-N) 3-Phase AC and 270 Vdc input power.

Continuous Power Rating

Steady-state output power is rated to 750 W for input line voltages above 100 Vrms (L-N). This is based on a rated output current of 27 A, providing design margin against the (maximum) 36 A current limit specification. As the steady-state output voltage is reduced for input line voltages below 100 Vrms (see Figure 10), the current rating and limits remain constant. Thus, the power rating is reduced proportionately as shown in Figure 14.

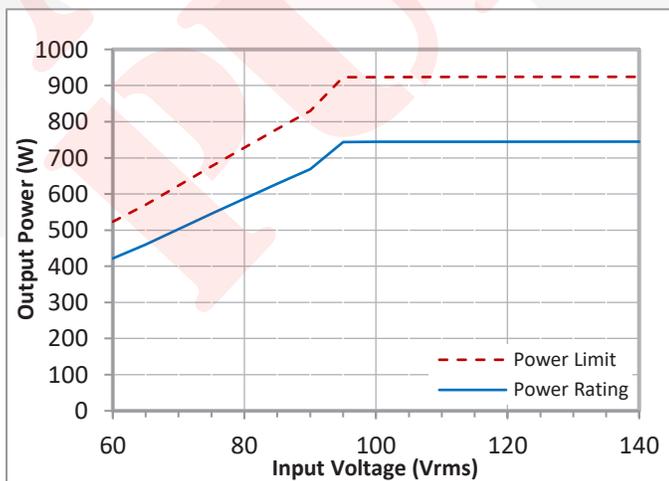


Figure 14: Steady-state rated and limit output power vs. AC line voltage.

Note that if the PFC output is driving DC-DC converters that exhibit constant-power characteristic at their inputs, the output voltage will collapse if the PFC's current limit is reached. The collapse rate would be governed by the external output capacitance value. It is therefore recommended to operate the converter at or below rated power in steady state, approaching current limit only during transient events.

POWER INTERRUPTS AND HOLDUP

Many systems need to operate through brief interruptions of AC input power. External capacitors placed at +VOUT can be used to maintain power flow to critical loads during these input power interruptions.

Holdup Capacitor Value

During a AC dropout of a given duration, the load is supplied from the bulk cap. The dropout is characterized by its energy.

$$E_{holdup} = P_{out} \cdot t_{drop}$$

where:

P_{out} is the output power during the holdup event

t_{drop} is the duration of the input power interruption

Based on this energy requirement, the holdup capacitor value is

$$C_{holdup} > \frac{2 \cdot E_{holdup}}{(V_s^2 - V_f^2)}$$

where:

V_s is the initial holdup capacitor voltage immediately before the input power interruption

V_f is the minimum capacitor voltage during the transient

V_f should be chosen to be above the minimum acceptable voltage for the loads attached.

The required value for C can become quite large if the PFC's entire load is to be maintained through long dropouts. In this case it may be valuable to partition the load into portions that need to be maintained and other portions that can be briefly interrupted.

External Capacitor Selection

Capacitors connected externally at +VOUT, the rating should be higher than the output voltage of the module used. Standard aluminum electrolytic capacitors have several significant drawbacks:

- 1) Narrow temperature ratings
- 2) Relatively high ESR at room temperature
- 3) Very high ESR at low temperature
- 4) Poor reliability at high temperature

Conductive polymer solid electrolytic capacitors solve all four of these problems at the expense of somewhat lower energy density:

- 1) Rated for full -55 °C to 125 °C temperature range
- 2) Good ESR at room temperature
- 3) Rated to maintain good ESR at low temperature
- 4) Much better reliability

PROTECTION FEATURES

Over-Temperature Shutdown

An internal sensor monitors the temperature of the PFC's PCB. If the sensor value exceeds 115 °C the **BATTLE SHORT** pin is released; if it exceeds 125 °C the unit will disable itself. At full-rated power this corresponds to a baseplate temperature of \approx 110 °C (higher at reduced load). The OTP shutdown can be disabled by externally holding the **BATTLE SHORT** pin low. When the internal temperature cools below 115 °C, **BATTLE SHORT** is internally driven low again and the PFC restarts automatically. See also the description of the **BATTLE SHORT** pin.

Input Phase Imbalance Shutdown

If the 3-phase AC input voltage should become excessively imbalanced (more than 35 Vrms amplitude or 18° angle imbalance), **AC GOOD** will be de asserted and **BATTLE SHORT** pin will be released. Input phase drop events also appear as excessive imbalance. The PFC will attempt to maintain power flow during this imbalance for 0.25 seconds before shutting down to protect itself, the load, and/or the source. This shutdown can be disabled by externally holding the **BATTLE SHORT** pin low. When the AC line voltage returns to normal limits, **BATTLE SHORT** will be internally driven low again and the PFC will restart automatically. See also the description of the **BATTLE SHORT** pin.

Short Circuit Current Limit

In most overload conditions, the linear output current limit is sufficient to protect the unit. A backup "short-circuit current limit" circuit, however, handles severe input transients or output short-circuit events. Redundant current sense resistors and comparators are connected in series with both the positive and negative sides of the buck PFC stage, set to trip well above the linear current limit threshold. When this backup protection is activated, the unit will respond by turning off all power flow from the input for approximately 200 μ s, after which normal operation resumes immediately.

Input Over-Voltage Protection

If the instantaneous voltage between any two line inputs goes above the threshold of 500 V (L-L), then all power flow from the input will be interrupted, resuming 1 ms after the input voltage falls again below the same threshold. (Voltage spikes shorter than 80 μ s may not trigger this protection response.) During an interruption, the output voltage will fall at a rate determined by output capacitance and load current.

Input Under-Voltage Shutdown

The input voltage must be above 100 Vrms (L-N) to activate **INPUT GOOD** and allow the unit to start up. If the input voltage subsequently drops below 50 Vrms (L-N) for more than 1 second the unit will shut down. The unit will stay off for at least 1 second.

Output Over-Voltage Protection

A redundant hardware over-voltage protection circuit will momentarily disable the PFC if the output ever rises more than 10% above its nominal value. The unit resumes normal operation immediately after the output voltage returns below this threshold.

Output Under-Voltage Shutdown

Should the action of the current limit reduce the output voltage to less than 25% of nominal for more than 150 ms, the unit will assume a sustained overload and will shut down. Auto-restart will occur after 1 second. This feature is also present during startup and thus serves to limit energy delivered into a shorted output.

EMI RECOMMENDATIONS

Input Filtering

As shown in Figure A, it is recommended to pair the PFC module with the separately available MACF-115-3PH-UNV-QG quarter brick 3-phase AC input filter module.

An external common-mode capacitor, shown in Figure A as C_{cm} , is also recommended. The typical value for C_{cm} is 47nF; route it as directly as possible from the MPFIC output to the PE GND pin of the input EMI filter and the baseplates of both the EMI Filter and the MPFIC unit.

Conducted Emissions Measurements

The MPFIC-115-3PH-28R-FT, 28 V PFC module paired with an MACF-115-3PH-UNV-QG, 3-Phase AC input line filter on an was demonstrated to pass MIL-STD-461 CE101 and CE102 requirements as shown below.

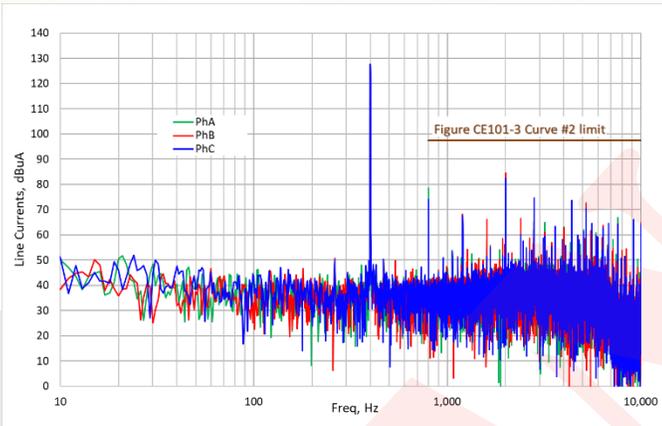


Figure 15: CE101 data at 400Hz, 750W output power, (3-phases)

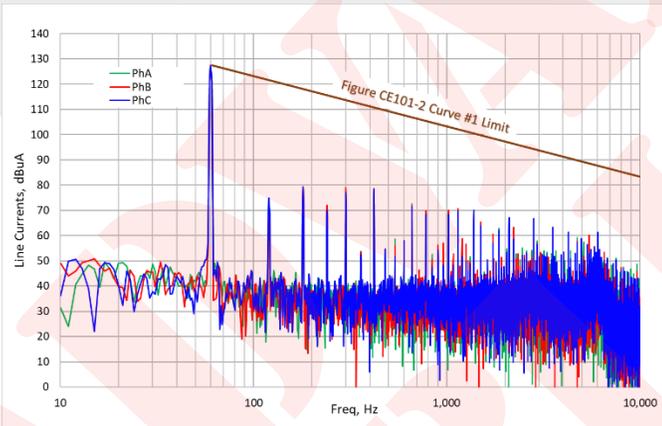


Figure 16: CE101 data at 60Hz, 750W output power, (3-phases)

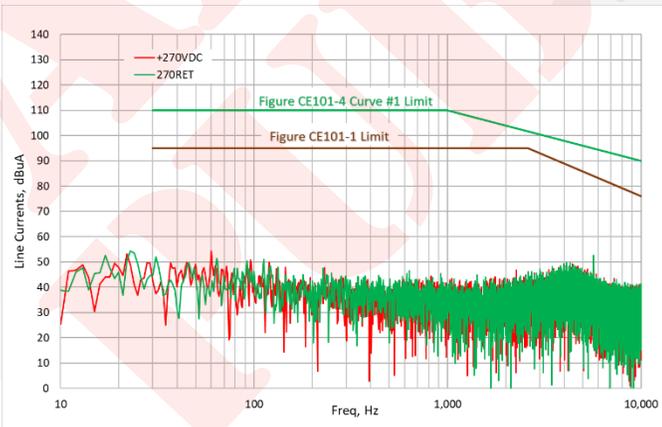


Figure 17: CE101 data at 270VDC in, 750W output power, (+270V and 270V RTN)

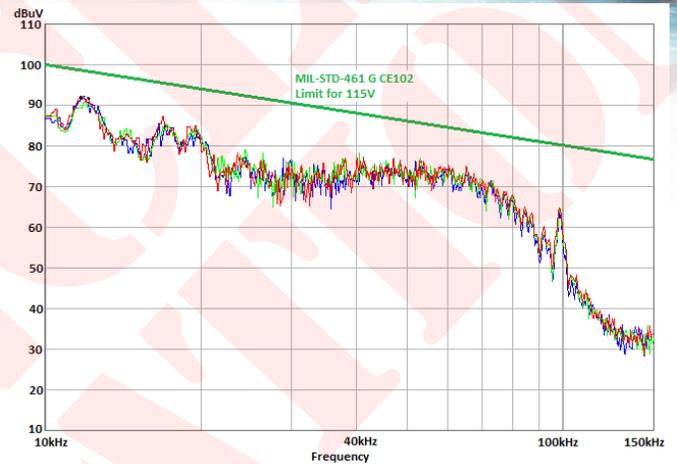


Figure 18: CE102 data at 400 Hz, 750W output power, 10kHz to 150kHz (3-phases)

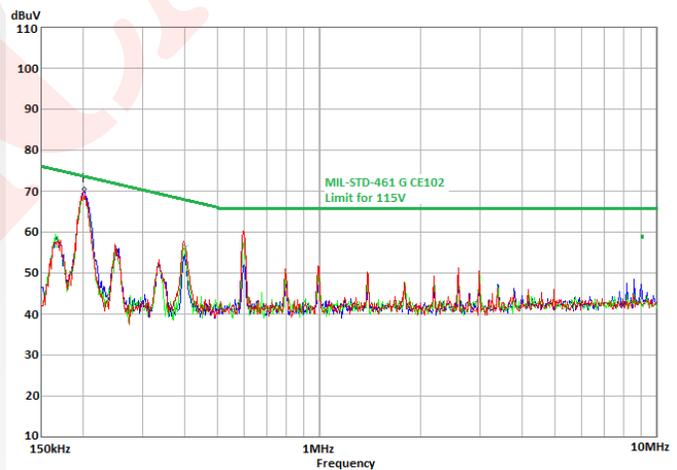


Figure 19: CE102 data at 400 Hz, 750W output power, 150kHz to 10MHz (3-phases)

Input Protection

The input stage implemented in this module offers far better immunity from input surges than a traditional boost topology. In a traditional boost PFC, there is no mechanism to limit current flow directly from input to output during operation, so for long duration surges, the current becomes very large and results in permanent destruction. In contrast, the buck PFC input stage used in this module is able to interrupt current flow during a voltage surge which dramatically lowers device stresses.

The PFC input lines, however, must be protected from spikes which might exceed their 575 V_{pk} (L-L) absolute-maximum rating. It is recommended to add external protection devices directly between the three pairs of PFC line input pins. Figure A shows an example input protection circuit consisting of clamping devices connected line-line in a “delta” configuration,

one set before and one set after the external MACF-115-3PH-UNV-QG input filter module. The set of Metal Oxide Varistors (MOVs) upstream of the filter prevent local arcing during a surge event due to input wiring inductance. These MOVs have a “soft” breakdown characteristic: at high currents they will clamp at a relatively high voltage. The set of special TVS devices downstream of the filter module have far superior characteristics. These AK3-430C devices made by Littlefuse (or equivalent Bourns PTVS-430C-TH) have superb clamping voltage: even at high currents they hold the input voltage below the 575 Vpk (L-L) absolute maximum specification of the PFC module. These devices also have high energy capability: whereas standard TVS devices have a relatively small die, the AK3 series parts have many large dies stacked on top of each other. This allows the AK3 to withstand very high energy repetitive transients without damage. Protection devices in the end user application should be tailored to the expected surge requirements. Fuses rated for 10 A are recommended in series with each input line, located upstream of the MOVs.

Baseplate Electrical Connection

All circuitry in the PFC module is electrically isolated from the baseplate with a multi-layer solid insulator. This isolation barrier meets basic insulation requirements and is 100% hi-pot tested in production to 1500 Vrms. The baseplate and corner mounting posts may therefore be connected to protective earth ground in the application circuit. Maintain adequate clearance from all external circuitry to the four corner mounting posts, which are electrically connected to the baseplate.

Safety Notes

The PFC provides reinforced isolation across its input and output terminal pins. Care must be taken to avoid contact with primary-side voltages, as well as with the AC source voltage.

The MPFIC must have an input current limiting device. The Technical Application diagrams show fuses used in series with the AC or DC source.

CONTROL PINS

START SYNC (Pin A1)

Pin A1 is designated as START SYNC, and is only implemented on the Droop model. This pin is not used on the Regulated-output model and should be left floating when not used. In paralleled applications, connect START SYNC between multiple units to synchronize restart after a fault condition. Internal interface circuitry is shown in Figure 24.

CTL RETURN (Pin A2)

CTL RETURN serves as the ground reference for all control signals. 3 kV of reinforced isolation is provided between all control pins and the power pins. CTL RETURN may be

externally connected to any of the power pins, attached to an application circuit, or left floating.

SERIAL IN (Pin A3)

A wide variety of operating parameters (voltages, currents, temperatures) may be accessed via the built-in full-duplex asynchronous serial interface. Commands may be transferred to the internal DSP via the SERIAL IN pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). A ‘start’ or ‘zero’ bit is encoded as a logic low. The internal baud rate will be exactly 20.48 times slower than the SYNC OUT frequency. The tolerance of both frequencies is better than +/- 2%. The frequency tolerance of the external interface circuit should also be better than +/- 2% accuracy to ensure that the last bit of incoming serial data arrives within the proper frame time. Alternatively, the SYNC OUT signal may be used to continuously calibrate the baud rate of the external interface circuit, allowing the use of a less-accurate oscillator.

The SERIAL IN pin may be left open if unused, and will be internally pulled up to 3.3V AUX, corresponding to the ‘idle’ or ‘stop’ state. Internal circuitry is shown in Figure 20. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive from a standard RS-232 port (see evaluation board schematic). See the separate “SynQor 3-Phase Input PFC Serial Interface” companion document for detailed command syntax (available at www.synqor.com/3-Phase Input PFC Serial Interface).

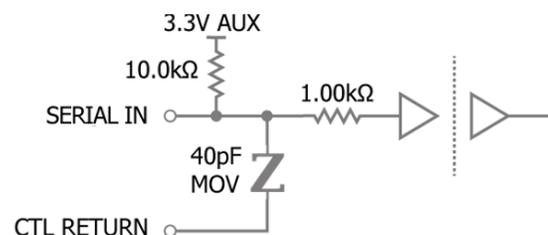


Figure 20: Internal circuitry for SERIAL IN pin.

SERIAL OUT (Pin A4)

A response to each command is sent via the SERIAL OUT pin at 9600 baud (8N1 – 8 data bits, no parity, 1 stop bit). The output is low for a ‘start’ or ‘zero’ bit. When not transmitting, the output is high, corresponding to the ‘idle’ or ‘stop’ state. Internal circuitry is shown in Figure 25. Direct connection may be made to an external microcontroller, but an external transceiver IC is required to shift levels and polarity to drive a standard RS-232 port (see evaluation board schematic). See the separate “SynQor 3-Phase Input PFC Serial Interface” companion document for detailed command syntax (available at www.synqor.com/3-Phase Input PFC Serial Interface).

INPUT GOOD (Pin A5)

The unit will not turn on until the positive-logic INPUT GOOD output is high, typically for line inputs between 96 Vrms (L-N) and 148 Vrms (L-N), or 220 to 340 Vdc. When the unit is already running, the INPUT GOOD output will typically transition low when the input voltage (at the PFC input pins) goes below 95 Vrms (L-N) or 235 Vdc, or above 149 Vrms (L-N), 340 Vdc. Instantaneous line-to-line voltage measurements are used, so these voltage thresholds will be affected by imbalance in line phase and/or amplitude.

INPUT GOOD also responds to input line frequency. If the input line frequency goes above 900 Hz, INPUT GOOD will transition low.

INPUT GOOD generally only serves as a power interruption warning: the unit will continue to run if INPUT GOOD transitions low, the only exception being an excessive input phase imbalance. During the imbalance, the PFC will attempt to maintain power flow for 0.25 seconds before shutting down to protect itself, the load, and/or the source, unless this function is overridden by BATTLE SHORT (see "Input Phase Imbalance Shutdown" section).

The response time of INPUT GOOD to an input power interruption is less than 1 ms at 400 Hz and less than 5 ms at 60 Hz. INPUT GOOD will return to its normal high state 20 ms after the line voltage recovers. Internal interface circuitry is shown in Figure 21.

DC GOOD (Pin A6)

During startup the positive-logic DC GOOD output will remain low until +VOUT crosses the rising threshold value (see Figure 22). The falling threshold is significantly lower, such that DC GOOD will usually remain high during an input power interruption. Therefore, DC GOOD is typically used to indicate successful startup, whereas AC GOOD is used to warn of an input power interruption. The typical DC GOOD response time is less than 1 ms. Internal interface circuitry is shown in Figure 21.

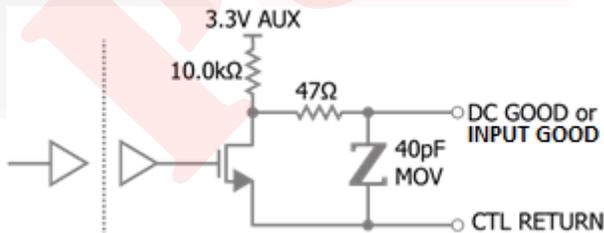


Figure 21: Internal circuitry for INPUT GOOD and DC GOOD pins.

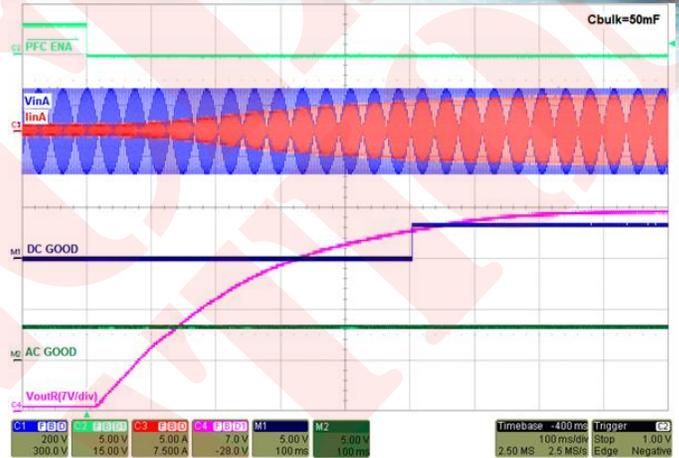


Figure 22 Timing from PFC ENA to startup and DC GOOD, VinA and IinA also shown for reference.

PFC ENA (Pin A7)

The PFC ENA pin must be brought low to enable the unit. A 10.0 kΩ pull-up resistor is connected internally to 3.3V AUX. Therefore, if all control pins are left floating, the unit will be disabled. The delay from enable to the beginning of the startup ramp is typically 30 ms (see Figure 22). Internal interface circuitry is shown in Figure 23.

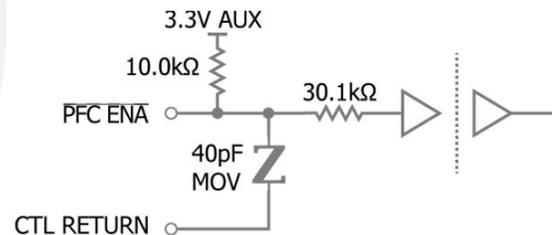


Figure 23: Internal circuitry for PFC ENA pin.

BATTLE SHORT (Pin A8)

The BATTLE SHORT pin, see Figure 24Figure 23, is both an input and an open drain output, pulled to 3.3V AUX through 10kΩ resistor. Under all normal operating conditions the PFC drives/holds the BATTLE SHORT pin low. The user can read this low level as an indication of normality.

If, however, the unit warms to within 10°C of Over Temperature Shutdown, or senses excessive phase imbalance (including a phase dropout), the BATTLE SHORT pin is released. Undriven, the pin will be pulled to 3.3V AUX and the user can read this high level as an indication of impending shutdown. If the unit continues to warm, or if the phase imbalance persists for more than 250ms, the module will read the BATTLE SHORT pin level. If it is high, the unit will shut down to protect itself. If, on the other hand, the BATTLE SHORT pin is externally held low when read, the module will continue to operate, potentially to destruction.

Technical Specification

If $\overline{\text{BATTLE SHORT}}$ action is always desired, the pin can simply be externally tied low.

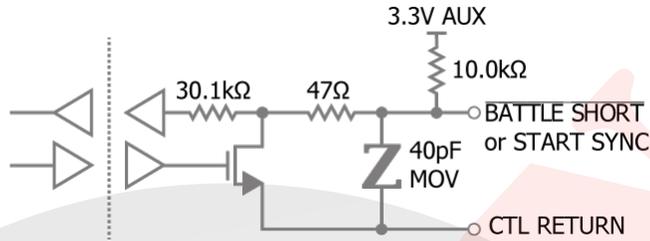


Figure 24: Internal circuitry for $\overline{\text{BATTLE SHORT}}$ and START SYNC pins.

3.3V AUX (Pin A9)

The 3.3V AUX supply (relative to CTL RETURN) can source up to 100 mA to power user loads. This independent supply is always energized whenever AC input voltage is present. In addition, during AC Line interruptions, this supply runs from energy stored in external bulk capacitance at VOUT (providing that the PFC was operating prior to the line interruption and that the voltage at VOUT remains >50% of nominal until AC power returns).

If unused, the 3.3V AUX output should be left open.

SYNC OUT (Pin A10)

The SYNC OUT pin generates a continuous series of pulses at the main switching frequency. The buck and boost converters are synchronized and switch at the same frequency. The SYNC OUT pin may be left open if not used. Internal interface circuitry is shown in Figure 25.

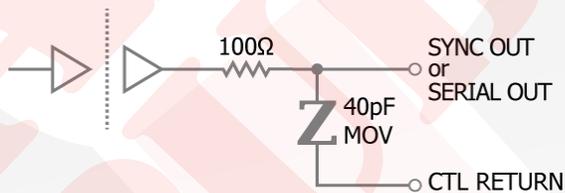
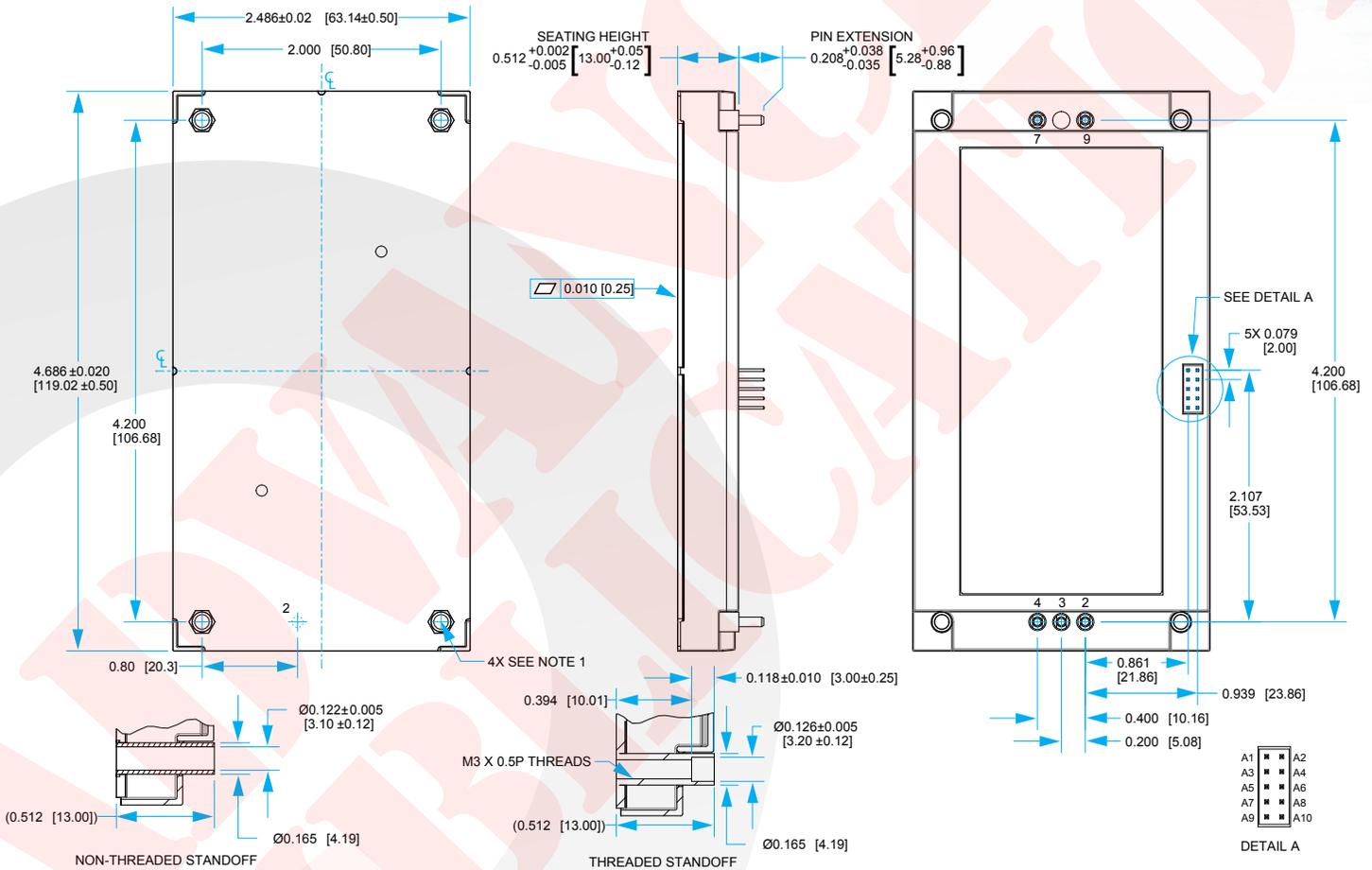


Figure 25: Internal circuitry for SYNC OUT and SERIAL OUT pins.



NOTES:

1. APPLIED TORQUE PER M3 SCREW SHOULD NOT EXCEED 6 in-lb (0.7 Nm)
2. BASEPLATE FLATNESS TOLERANCE IS 0.010" (0.25 mm) TIR FOR SURFACE.
3. PINS 2-4, AND 7, AND 9 ARE 0.080" (2.03 mm) DIA. WITH 0.125" (3.18 mm) DIA. STANDOFF SHOULDERS
MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
4. PINS A1-A10 ARE 0.020" X 0.020" (0.51mm X 0.51mm)
MATERIAL: PHOSPHOR BRONZE, FINISH: GOLD FLASH OVER NICKEL UNDERPLATING.
5. THREADED OR NON-THREADED OPTIONS AVAILABLE
6. UNDIMENSIONED COMPONENTS ONLY FOR VISUAL REFERENCE
7. ALL DIMENSIONS IN INCHES (mm)
TOLERANCES: X.XX IN +/-0.020 (X.X mm +/-0.5 mm)
X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
8. WEIGHT: 10.0 oz (284 g)

PIN DESIGNATIONS

Pin	Label	Name	Function
2	LINE A	LINE A	AC Line A Input
3	LINE B	LINE B	AC Line B Input
4	LINE C	LINE C	AC Line C Input
7	-VOUT	VOUT(-)	Negative Return for +VOUT
9	+VOUT	VOUT(+)	Positive Boost Output Voltage
A1	RESERVED	RESERVED	No Connect
A2	CTL RETURN	CTL RETURN	Isolated Ground Reference for Pins A1 - A10
A3	SERIAL IN	SERIAL IN	Serial Data Input (High = Stop/Idle)
A4	SERIAL OUT	SERIAL OUT	Serial Data Output (High = Stop/Idle)
A5	INPUT GOOD	INPUT GOOD	Input Power Good Output (High = Good)
A6	DC GOOD	DC GOOD	DC Power Good Output (High = Good)
A7	PFC ENA	PFC ENA	Pull Low to Enable Unit
A8	BATTLE SHORT	BATTLE SHORT	Pull Low to Disable OTP / Phase Drop Shutdown
A9	3.3V AUX	3.3V AUX	3.3V @ 100mA Always-On Power Output
A10	SYNC OUT	SYNC OUT	Switching Frequency Synchronization Output



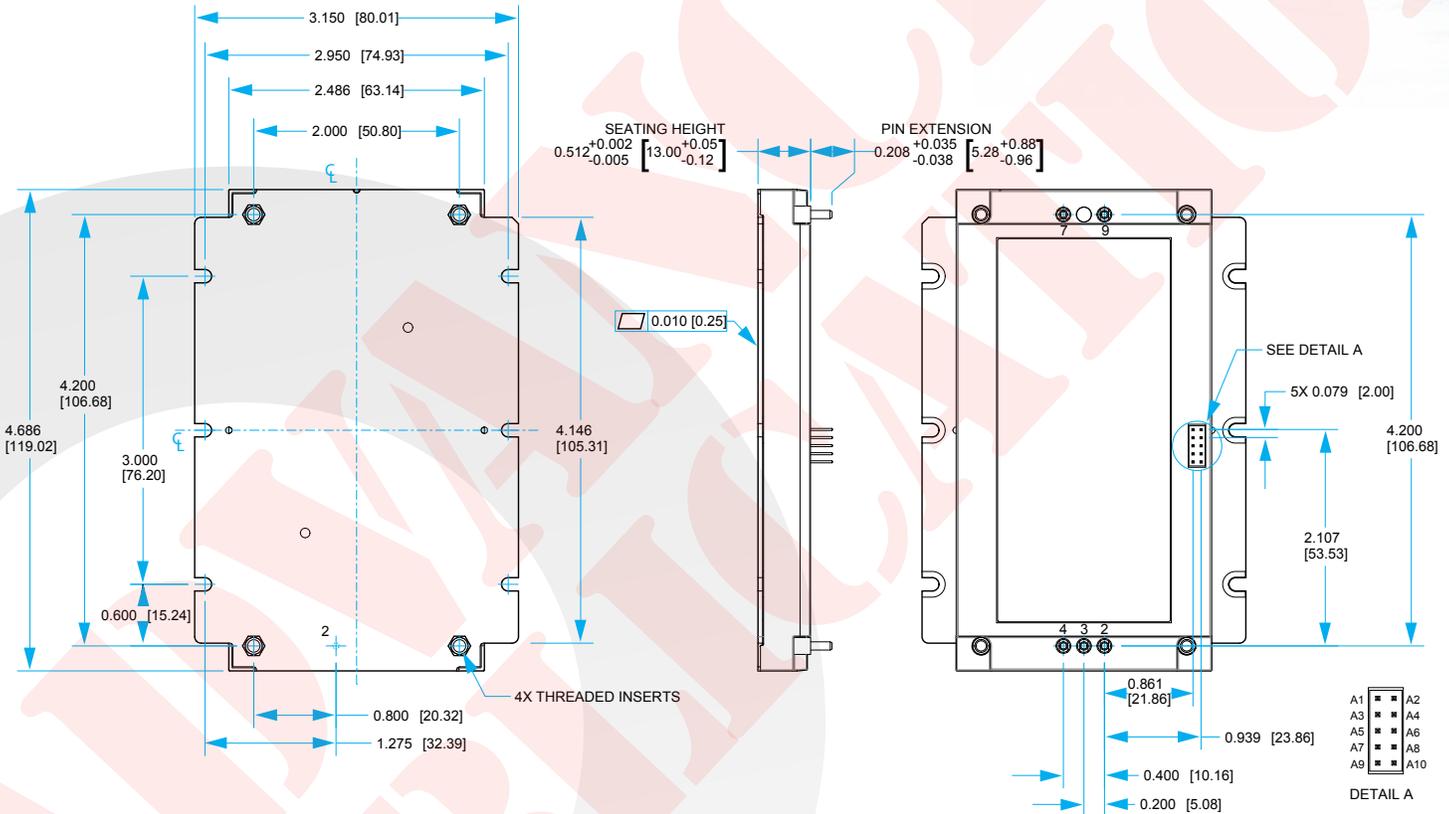
Encased Mechanical with Flange

MPFIC-115-3PD-28x-FT

Input: 3Φ 115Vrms (L-N) or 270 Vdc

Output: 28 Vdc

Power: 750W



NOTES:

1. APPLIED TORQUE PER M3 OR 4-40 SCREW SHOULD NOT EXCEED 6 in-lb (0.7 Nm)
2. BASEPLATE FLATNESS TOLERANCE IS 0.010" (0.25 mm) TIR FOR SURFACE.
3. PINS 2-4, 7 AND 9 ARE 0.080" (2.05 mm) DIA. WITH 0.125" (3.18 mm) DIA. STANDOFF SHOULDERS. MATERIAL: COPPER ALLOY. FINISH: MATTE TIN OVER NICKEL PLATE.
4. PINS A1-A10 ARE 0.020" X 0.020" (0.51mm X 0.51mm) MATERIAL: PHOSPHOR BRONZE, FINISH: GOLD FLASH OVER NICKEL UNDERPLATING
5. UNDIMENSIONED COMPONENTS ONLY FOR VISUAL REFERENCE
6. ALL DIMENSIONS IN INCHES (mm)
TOLERANCES: X.XX IN +/-0.020 (X.X mm +/-0.5 mm)
X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
X.XXX IN +/-0.010 (X.XX mm +/-0.25 mm)
7. WEIGHT: 10.3 oz (290 g)

PIN DESIGNATIONS

Pin	Label	Name	Function
2	LINE A	LINE A	AC Line A Input
3	LINE B	LINE B	AC Line B Input
4	LINE C	LINE C	AC Line C Input
7	-VOUT	VOUT(-)	Negative Return for +VOUT
9	+VOUT	VOUT(+)	Positive Boost Output Voltage
A1	RESERVED	RESERVED	No Connect
A2	CTL RETURN	CTL RETURN	Isolated Ground Reference for Pins A1 - A10
A3	SERIAL IN	SERIAL IN	Serial Data Input (High = Stop/Idle)
A4	SERIAL OUT	SERIAL OUT	Serial Data Output (High = Stop/Idle)
A5	INPUT GOOD	INPUT GOOD	Input Power Good Output (High = Good)
A6	DC GOOD	DC GOOD	DC Power Good Output (High = Good)
A7	PFC ENA	PFC ENA	Pull Low to Enable Unit
A8	BATTLE SHORT	BATTLE SHORT	Pull Low to Disable OTP / Phase Drop Shutdown
A9	3.3V AUX	3.3V AUX	3.3V @ 100mA Always-On Power Output
A10	SYNC OUT	SYNC OUT	Switching Frequency Synchronization Output



SynQor®

Ordering Information

MPFIC-115-3PD-28x-FT
Input: 3Φ 115Vrms (L-N) or 270 Vdc
Output: 28 Vdc
Power: 750W

Part Numbering Scheme						
Family	Input Voltage	Output	Regulation	Package Size	Thermal Design	Screening Level
MPFIC	115-3PD: 3-Phase 115 Vrms L-N	28: 28V	R: Regulated output D: Droop Sharing	FT: Full-brick Tera	N: Normal Threaded D: Non-Threaded F: Flanged Baseplate	S: S-Grade M: M-Grade

Example:MPFIC-115-3PD-28D-FT-N-M
MPFIC-115-3PD-28R-FT-N-M

PART NUMBERING SYSTEM

The part numbering system for SynQor's ac-dc converters follows the format shown in the example.

APPLICATION NOTES

A variety of application notes and technical white papers can be downloaded in PDF format from our [website](#).

Parameter	Notes & Conditions
STANDARDS COMPLIANCE	Pending
Input/Output to baseplate isolation 2150Vdc	Basic Insulation to Baseplate
CE Marked	
SELV DC Output	Reinforced Insulation

Note: An external input fuse must always be used to meet these safety requirements.
 Contact SynQor for official safety certificates on new releases or download from the SynQor website.

Contact SynQor for further information and to order:

Phone: 978-849-0600 **Fax:** 978-849-0602
E-mail: power@synqor.com **Web:** www.synqor.com
Address: 155 Swanson Road, Boxborough, MA 01719 USA

WARRANTY

SynQor offers a two (2) year limited warranty. Complete warranty information is listed on our website or is available upon request from SynQor.

PATENTS

SynQor holds numerous U.S. patents, one or more of which apply to most of its power conversion products. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S. patent laws. SynQor's patents include the following:
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