

Advancing The Power Curve

Thermal & Reliability Study on High **Current Thermal Vias & Output Pins**

Application Note 00-08-01 Rev. 03 - 7/31/01



Summary:

This application note addresses concerns raised with regards to pin and board heating when high currents (≥60A) are driven through thermally relieved plated through hole (PTH) vias. Detailed thermal analysis will show that internal heat generation and resulting temperature rise of the power converter and load board is minimal when using a single thermally relieved via.

Introduction

Trends in the design of Distributed Power Architectures (DPA's) are requiring DC-DC converters to deliver very high power at very low voltages. This has required a thorough examination on how high current power can be delivered safely and reliably to the distribution path within a printed circuit card. SynQor has evaluated these challenges through theoretical analysis and carefully controlled laboratory testing. Using the latest in thermal imaging equipment as well as analytical calculations, SynQor has concluded that currents in excess of 60A can be safely and reliably delivered through a single pin. In addition, SynQor demonstrates that reasonable thermal relief geometries do not have significant self heating at 60A.

1.0 Pin Resistance

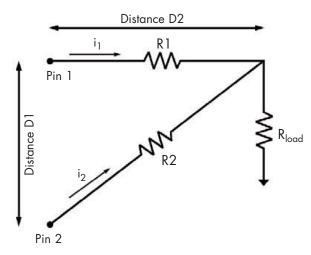
The first concern is that the resistive loss in a single output pin might contribute excessively to power losses in the distribution path or create a severe temperature rise within the pin due to self heating from I-R losses. It is relatively simple to calculate the resistance of a standard output pin. The measured resistance of SynQor's standard 0.080" brass output pin is 0.14mΩ. Using Equation 1 the total power dissipated within a pin delivering 60A is 0.504W. From these equations we can see that the power dissipation is relatively small when compared to the total power dissipation in the unit when delivering 60A. The efficiency and power dissipation specified in SynQor's data sheets includes the effect of pin resistance. The pin temperature increase, albeit small, is factored into the power derating curves on the data sheet, since the thermal connection between the pin and the SynQor PC board is very good. It should also be noted that the total voltage drop across both output pins is about 16mV, which is likely much smaller than the further copper distribution losses.

 $P_{diss} = I^2 R$ Equation 1:

2.0 Multiple Output Pins and Distribution Losses

Another common assumption is that by having multiple output pins, power losses will be reduced in the distribution path due to an overall decrease in the distribution path resistance. This is true for the circuit as drawn in Figure 1, where R1 and R2 represent the distribution losses in a circuit card, and distance D1 is similar to distance D2. In this situation the total losses are calculated in Equation 2. Table 1 shows that two pins with half the current spaced far enough apart can have a much lower power loss than 1 pin carrying the same current.

Equation 2: Total Power Lost Figure $1 = i_1^2 *R1 + i_2^2 *R2$



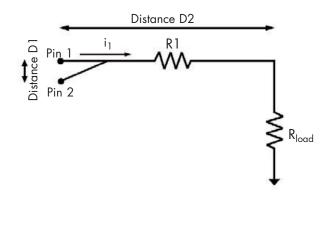


Figure 1: Converter layout with 2 output pins spaced far apart (non-practical)

Figure 2: Converter layout with 2 output pins spaced close together (typical)

For a typical circuit card and converter however, the distance D1 is much smaller than D2 as shown in Figure 2, and hence the overall power loss is given by equation 3. Two output pins placed closely together offers no advantage if the distance between the pins is small compared to the size of the distribution path, as is the case for all commercially available converters.

Total Power Lost Figure $2 = i_1^2 R1$ Equation 3:

Circuit	I ₁	R1	l ₂	R2	P _{diss}
Figure 1	30A	0.5 m Ω	30A	$0.7 m\Omega$	1.10W
Figure 2	60A	0.5 m Ω	0	0	1.80W

Table 1: Dissipated Power of circuits from Figures 1 & 2.

3.0 Thermal Relief Designs and Power Loss - Predicted

Another challenge facing today's power designer is the use of thermal reliefs in the design of high current Printed Circuit Boards (PCB's). Standards in the design of high reliability circuit packs require that designers use thermal reliefs to insure reliable solder connections between converter pins and the circuit card during the soldering process. The use of these thermal reliefs are often viewed as highly resistive elements that can contribute to significant self heating within a circuit card, especially if only one pin is available to deliver current. Through calculation and detailed analysis of thermal images taken in SynQor's laboratory, SynQor demonstrates that a properly designed thermal relief does not create a reliability concern due to self heating within the thermal relief. The data clearly shows that while there is a thermal gradient from the hotter converter board to the cooler customer board, there is very little heating due to the resistance of the spokes in the thermal relief.

Theoretical Analysis

In order to find the heat generated in a conductor when current passes through it, the resistance of the conductor must be known. The resistance is defined by the Equation 4.

Equation 4
$$R = length/(\sigma r^*width^*thickness)$$
 where $[\sigma r]$ is 50 E6 amps²/Watt·meter for copper, and the geometry pertains to a conductor with a rectangular cross-section.

The heat generated is $[i^2R]$, so the heat generation per unit volume $[Qdot_V''']$ of the conductor is $[i^2R/(area^*length)]$. For a conductor with a rectangular cross section, $[A=w^*t]$, so:

Equation 5
$$Qdot_{v'''} = i^2/(\sigma_r * w^2 * t^2)$$

For a small length $[\Delta x]$ of the conductor, the rate of heat transfer into the system boundary minus the heat transfer out of the system boundary plus the heat generated within the system must equal zero.

Equation 6
$$Qdot_{X}-Qdot_{X+\Delta X}+i^2/(\sigma_r^*w^2*i^2)^*\Delta x^*t^*w=0$$

Dividing both sides by $[\Delta x]$ and allowing $[\Delta x]$ to approach zero yields:

Equation 7
$$dQdot/dx = i^2/(\sigma_r^*w^*t)$$

Substituting the heat flux times the area for [Qdot] (Fourier's Law), and dividing both sides by [w*t*k],

Equation 8
$$d/dx[dT/dx] = i^2/(\sigma_r^*w^2*t^2)/(-k)$$

where the thermal conductivity [k] is 386 Watts/meter°C for copper.

Integrating once reveals

Equation 9
$$dT/dx = i^2/(\sigma_r^* w^2 * t^2)/(-k)^* x + C1$$

A second integration gives us the following:

Equation 10
$$T(x) = i^2/(\sigma_r^* w^2 * l^2) * x^2/(2*(-k)) + C1*x + C2.$$

Our boundary conditions are that the temperature at [x=0] is the pin temperature $[T_{pin}]$ and that the temperature at [x=l] is the load board temperature $[T_{board}]$. When [x=0], [T(x)] = [C2], so [C2] is equal to $[T_{pin}]$. Setting [T(l)] equal to $[T_{board}]$ gives the following solution for [C1].

Equation 11 C1 =
$$(T_{board} - T_{pin} - (i^2 * l^2)/(2 * l^2 * w^2 * \sigma_r * (-k)))/l$$

Combining Equations 10 and 11 gives the generalized solution for the temperature as a function of the position along the spoke length.

Equation 12
$$T(x) = i^2 x^2/(2 \sigma_r^* w^2 t^2 (-k)) + (T_{board} - T_{pin} - (i^2 t^2)/(2 t^2 w^2 \sigma_r^* (-k))) x / l + T_{pin}$$

If Equation 12 is rearranged, the temperature along the length of the spoke becomes the superposition of a linear change in temperature between the pin and board plus a length dependent increase in temperature due to the i²R heating.

Equation 13
$$T(x) = T_{board} * x/l + T_{pin} * (1-x/l) + i^2/(2*\sigma_r * w^2*l^2*(-k))*(x^2-l*x)$$

This shows that the [i²] term is independent of the pin and board temperatures, and the [i²R] heating term can now be calculated directly.

Equation 14 Temperature Rise Due to i²R Heating in the Spokes of a Thermal Via as a Function of Length

$$\Delta T = i^2/(2 * \sigma_r * w^2 * t^2 * (-k)) * (x^2 - l * x)$$

Where the maximum temperature increase will be at the center of the spoke [x = 1/2]. Substituting $[\gamma]$ for the aspect ratio of the spokes $[\gamma=l/w]$,

Equation 15 Maximum Temperature Rise Due to i²R Heating in a Thermal Via Spoke

$$\Delta T = i^2 \gamma^2 / (8 * \sigma_r * t^2 * k)$$

Example 1: Internal Heat Generation in a Typical Thermal Via

A typical thermally relieved via has 4 spokes with an aspect ratio [γ] of 0.6 (15 mil length, 25 mil trace width). If a circuit board has only one copper plane with a thickness of 2 ounces [t=66E-6 m] and 60 amps is driven through one thermal via (15 amps per spoke), Equation 16 predicts a temperature increase at l/2 of 0.12° C.

$$\Delta T(l/2) = 15^2 * 0.6^2 / (8 * 50 E6 * (66 E - 6)^2 * 386) = 0.12 ° C$$

Example 2: Temperature Drop Due to Internal Heat Generation in a Severe Thermal Via

Consider an extreme example where a thermally relieved via has four spokes of one ounce copper [t=33E-6 m], and the spokes are twice as long as they are wide [γ =2]. Using Equation 16, the temperature increase at the center of the spoke when 60 amps is driven through the pin (15 amps per spoke), is 5.36°C.

$$\Delta T(1/2) = 15^2 * 2^2 / (8 * 50E6 * (33E-6)^2 * 386) = 5.36 °C$$

In this extreme case, a temperature rise of 5.36°C is expected at the center of the spoke due to i²R heating.

The heat generation within a typical thermal via is not expected to create a significant temperature rise, even with 60 amps delivered through one via. However, the squared dependence of heat generation on both the aspect ratio and reciprocal of the thickness of the thermal spokes makes it possible to design a thermal via that does create a modest temperature increase.

4.0 Thermal Relief Designs and Power Loss - Observed

To verify the above predictions an evaluation board was designed by SynQor such that the thermal characteristics of four different thermal reliefs could be observed. The thermal evaluation board (TEB) is documented as SynQor part number 031-1000026 Rev 1. The thermal reliefs vary in the length-to-width aspect ratio or scale of the spokes. The designed and measured geometry of the thermal relief spokes is listed in Table 2, see Figure 3 for the dimensioning key.

Via #	Length (designed/measured)	Width (designed/measured)	Aspect Ratio (length/width)
Via 1	0.040/0.044	0.060/0.067	2:3
Via 2	0.060/0.067	0.060/0.067	1:1
Via 3	0.060/0.067	0.090/0.095	2:3
Via 4	0.080/0.085	0.060/0.065	4:3

Table 2: Details of Thermal Relief Spokes

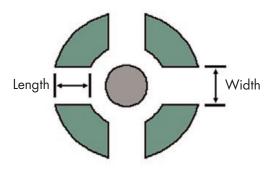


Figure 3: Thermal Relief Dimensioning Standard

Two 2.5V, 60A half-brick PowerQor Tera converters, SynQor part# PQ48025HTA60NKS were each solder mounted to a TEB. The spokes of the output thermal reliefs were severed on the side of the TEB to which the board was mounted. This was done so that all current would flow through the observable spokes on the opposite side. The copper is specified to be one ounce, plated to two ounces. The spokes were monitored with a thermal imaging camera while the 2.5 volt power converters delivered 60 amps at 25°C. Airflow was 300 LFM, airflow direction was from the output pins towards the input pins. Still images were captured with an infrared camera after the power converter and TEB reached steady state temperature. Close up thermal images of each sample were recorded, and from those images a plot was made detailing the spoke temperature in °C as a function of distance from the center of the pin outwards measured in pixels. By analyzing the second derivative of the temperature versus distance graphs, we are able to determine if heat is being generated within the spokes of the thermal relief. While the first derivative is an indication of the slope, the second derivative is an indicator of the "curve" within the line. Essentially a curved line shows self-heating within the spoke, i.e. the temperature increases as you go away from the pin.

Images 1 and 3, are two thermal reliefs with an aspect ratio of 2:3 (L:W). There is only negligible change between the two thermal images with a spoke aspect ratio of 2:3, which supports our derivation that only the thickness and aspect ratio of thermal relief spokes determine the thermal performance of a via. The image with a spoke aspect ratio of 1:1 (Image 2) is similar to those with an aspect ratio of 2:3. Plots 1, 2, and 3 show plotted data of Temperature versus Distance for the various thermal reliefs. As expected, each of these graphs show an almost linear temperature reduction as you move further out from the pin, indicating that there is no self heating within the spokes of the relief.

There are two distinct differences between Image 4 and the others due to the 4:3 aspect ratio of the relief. The "hub" temperature is several degrees warmer, and the temperature within the thermal relief spokes is greatest at the mid-length of the spokes. The first observation indicates that the increased aspect ratio of the spokes prevents heat from conducting away from the center of the thermal relief. The second observation is evidence of noticeable i²R heating along the length of this geometry of spoke. Graphing the data from Image 4 yields the Plots 4 and 5. These graphs indicate strongly the self-heating of the poorly designed thermal via. The increase in temperature along the length of the spoke is on the order of 4 degrees, which is approximated with the following equation:

Equation 16
$$\Delta T_{midlength} = i^2 \alpha^2 / (t^2 \sigma_r \kappa)$$

where i is current in amps, alpha is the spoke aspect ratio, t is copper thickness, σ_r is the electrical conductivity of copper (50e6 A²/WM), and κ is the thermal conductivity of copper (386 W/mK). For the geometry with the long spokes,

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 $\Delta T_{midlength} = 15^2(4/3)^2/((7.1e-5)^2(50e6)(386)) = 4.1 degrees,$

as observed.

Thermal Images and Temperature Gradients

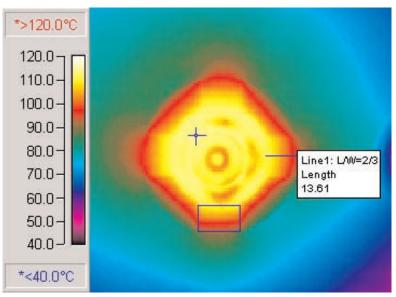
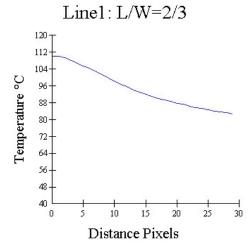


Image 1: Thermal image of Via #1 with a length/width aspect ratio of 2:3



Min 82.6°C, Mean, 94.6°C, Max 110.2°C, Std.Dev. 9.2°C, Length 30.0

Plot 1: Temperature gradient of Line 1 from Via #1 with a length/width aspect ratio of 2:3

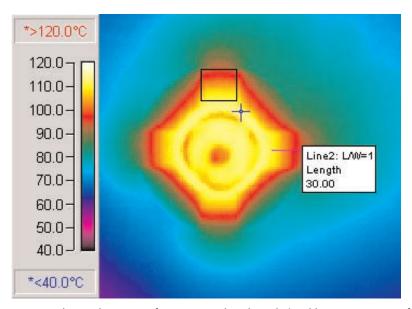
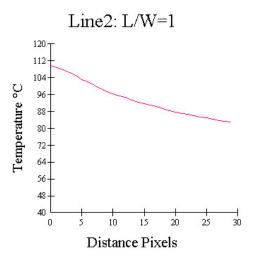


Image 2: Thermal image of Via #2 with a length/width aspect ratio of 1:1



Min 83.0°C, Mean, 93.8°C, Max 109.8°C, Std.Dev. 8.4°C, Length 30.0

Plot 2: Temperature gradient of Line 2 from Via #2 with a length/width aspect ratio of 1:1

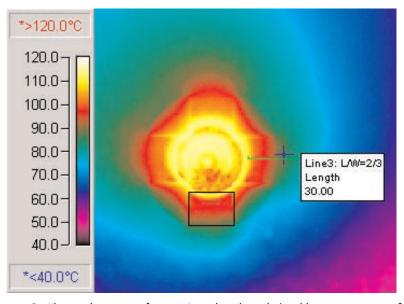
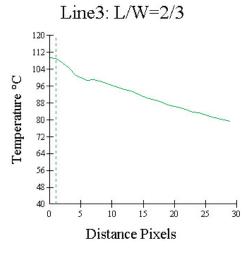


Image 3: Thermal image of Via #3 with a length/width aspect ratio of 2:3



Min 79.3°C, Mean, 92.3°C, Max 109.4°C, Std.Dev. 8.9°C, Length 30.0

Plot 3: Temperature gradient of Line 3 from Via #3 with a length/width aspect ratio of 2:3

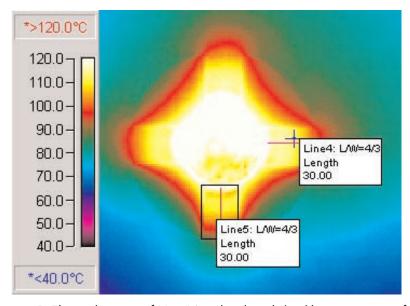
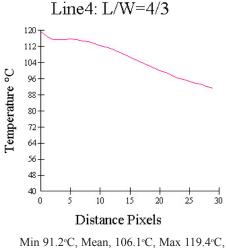
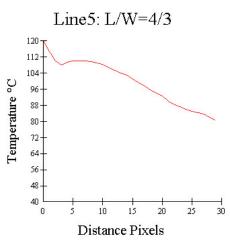


Image 4: Thermal image of Via #4 with a length/width aspect ratio of 4:3



Std.Dev. 8.9°C, Length 30.0



Min 80.6°C, Mean, 99.6°C, Max 120.0°C, Std.Dev. 11.3°C, Length 30.0

Plot 4: Temperature gradient of Line 4 from Via #4 Plot 5: Temperature gradient of Line 5 from Via #4 with a length/width aspect ratio of 4:3 with a length/width aspect ratio of 4:3



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